

EXHIBIT LL



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SPI Background

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History

SPI is a serial communication bus developed by Motorola. It is a full-duplex protocol that functions on a master-slave paradigm that is ideally suited to data stream application.

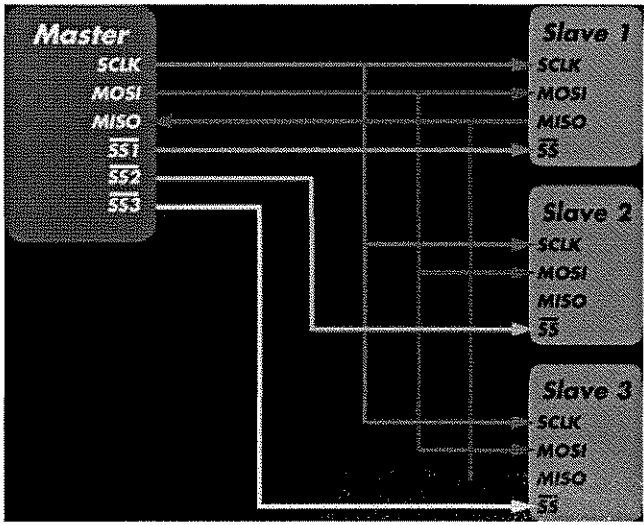
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Theory of Operation

SPI requires four signals: clock (SCLK), master output/slave input (MOSI), master input/slave output (MISO), slave select (SS).

Three signals are shared by all devices on the SPI bus: SCLK, MOSI and MISO. SCLK is generated by the master device and is used for synchronization. MOSI and MISO are the data lines. The direction of transfer is indicated by their names. Data is always transferred in both directions in SPI, but an SPI device interested in only transmitting data can choose to ignore the receive bytes. Likewise, a device only interested in the incoming bytes can transmit dummy bytes.

Each device has its own SS line. The master pulls low on a slave's SS line to select a device for communication.



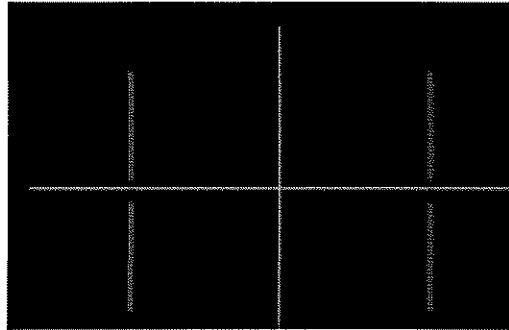
*Figure 1: Sample SPI implementation.
Each slave device requires a separate slave select signal (SS).*

The exchange itself has no pre-defined protocol. This makes it ideal for data-stream applications. Data can be transferred at high speed, often into the range of the tens of megahertz. The flip side is there is no acknowledgement, no flow control, the master may not even be aware of the slave's presence.

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Modes

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*Figure 2: SPI Modes
The frame of the data exchange is described by two parameters, the clock polarity (CPOL) and the clock phase (CPHA). This diagram shows the four possible states for these parameters and the corresponding mode in SPI.*

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Benefits and Drawbacks

SPI is a very simple communication protocol. It does not have a specific high-level protocol which means that there is almost no overhead. Data can be shifted at very high rates in full duplex. This makes it very simple and efficient in a single master single slave scenario.

Because each slave needs its own SS, the number of traces required is $n+3$, where n is the number of SPI devices. This means increased board complexity when the number of slaves is increased.

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References

- [Introduction to Serial Peripheral Interface](#) - Embedded.com
- [SPI - Serial Peripheral Interface](#)

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